REMARKS

Claims 1-20 are pending in the Application. Claims 1-18 and 20 are rejected under 35 U.S.C. §102(e). Claim 19 is rejected under 35 U.S.C. §103(a). Applicant respectfully traverses these rejections for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw these rejections.

Applicant notes that claims 6, 18 and 20 were not amended to overcome prior art but to be correct typographical errors. Hence, the amendments made to claims 6 and 18 were not narrowing in scope and therefore no prosecution history estoppel arises from the amendments to claims 6, 18 and 20. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendments made to claims 6, 18 and 20 were not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such amendments. *See Festo Corp.*, 62 U.S.P.Q.2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (1997).

Applicant thanks the Examiner for discussing the Office Action with Applicant's attorney on April 26, 2004, and in particular the rejections to claims 1 and 3.

I. REJECTIONS UNDER 35 U.S.C. §102(e):

Claims 1-18 and 20 have been rejected under 35 U.S.C. §102(e) as being anticipated by Zuraski Jr. et al. (U.S. Patent No. 6,502,188) (hereinafter "Zuraski"). Applicant respectfully traverses these rejections for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicant respectfully asserts that Zuraski does not disclose "shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken" as recited in claim 1 and similarly in claims 13 and 17. The Examiner cites column 12, lines 38-42; column 13, lines 7-36; Figures 4 and 5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 3. Applicant respectfully traverses asserts that Zuraski instead discloses that a taken branch is indicated by a binary one and a not taken branch is indicated by a binary zero. Column 13, lines 12-14. Zuraski further discloses that row A of Figure 4 shows the contents prior to dispatch of a conditional branch. Column 13, lines 17-18. Zuraski further discloses that row B of Figure 4 contains the contents after dispatch of a conditional branch. Column 13, lines 18-19. Zuraski further discloses that in this case, the conditional branch is predicted taken and a one is shifted into the register. Column 13, lines 19-21. Zuraski further discloses that row C of Figure 4 shows the contents after execution of the conditional branch. Column 13, lines 21-22. Hence, Zuraski discloses shifting a "1" in the shift register if the conditional branch is taken and shifting a "0" in the shift register if the conditional branch is not taken. However, Zuraski does not shift a "1" or a "0" in the shift register based on whether a group of instructions contains a branch instruction predicted as taken. Thus, Zuraski does not disclose all of the limitations of claims 1, 13 and 17, and thus Zuraski does not anticipate claims 1, 13 and 17. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken" as recited in claim 1 and similarly in claims 13 and 17. The Examiner cites column 12, lines 38-42; column 13, lines 7-36; Figures 4 and 5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 3. Applicant respectfully traverses. As stated above, Zuraski instead discloses that a taken branch is indicated by a binary one and a not taken branch is indicated by a binary zero. Column 13, lines 12-14. Zuraski further discloses that

row A of Figure 4 shows the contents prior to dispatch of a conditional branch. Column 13, lines 17-18. Zuraski further discloses that row B of Figure 4 contains the contents after dispatch of a single conditional branch. Column 13, lines 18-19. Zuraski further discloses that in this case, the conditional branch is predicted taken and a one is shifted into the register. Column 13, lines 19-21. Zuraski further discloses that row C of Figure 4 shows the contents after execution of the conditional branch. Column 13, lines 21-22. Hence, Zuraski discloses shifting a "1" in the shift register if the conditional branch is taken and shifting a "0" in the shift register if the conditional branch is not taken. However, Zuraski does not shift a "1" or a "0" in the shift register based on whether a group of instructions does not include a branch instruction predicted as taken. Thus, Zuraski does not disclose all of the limitations of claims 1, 13 and 17, and thus Zuraski does not anticipate claims 1, 13 and 17. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "indexing a branch history table using a first global history vector associated with a first fetch group of instructions during a first fetch cycle to retrieve a first prediction value" as recited in claim 6. The Examiner cites column 1, lines 12-32; column 12, lines 25-32 and Figure 3 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 4. Applicant respectfully traverses and asserts that Zuraski instead discloses that when a global branch is dispatched, a fetch address is conveyed to the local predictor storage, target array and line buffer. Column 12, lines 25-27. Zuraski further discloses that the fetch address is combined with the contents of the global history shift register to form an index which is conveyed to the global predictor storage. Column 12, lines 27-30. Thus, Zuraski discloses forming an index when a single global branch is dispatched. Zuraski does not disclose indexing a branch history table using a global history vector associated with a fetch group of instructions. Thus, Zuraski does not disclose all of the limitations of claim 6 and thus Zuraski does not anticipate claim 6. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "generating a second history vector associated with a second fetch group of instructions" as recited in claim

6. The Examiner cites column 13, line 37 to column 14, line 5 and Figures 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 4. Applicant respectfully traverses and asserts that Zuraski instead discloses an illustration of a mispredicted first conditional branch with a subsequent second conditional branch. Zuraski further discloses restoring the state of the global history shift register for conditional branch instructions improperly predicted. However, there is no language in the cited passages of generating a history vector associated with a fetch group of instructions. Thus, Zuraski does not disclose all of the limitations of claim 6 and thus Zuraski does not anticipate claim 6. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "appending a bit of a first value to the first vector when the first fetch group has at least one branch instruction predicted to be a branch taken" as recited in claim 6. The Examiner cites column 12, lines 38-42; column 13, lines 7-36; Figures 4 and 5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 4. Applicant respectfully traverses asserts that Zuraski instead discloses that a taken branch is indicated by a binary one and a not taken branch is indicated by a binary zero. Column 13, lines 12-14. Zuraski further discloses that row A of Figure 4 shows the contents prior to dispatch of a conditional branch. Column 13, lines 17-18. Zuraski further discloses that row B of Figure 4 contains the contents after dispatch of a conditional branch. Column 13, lines 18-19. Zuraski further discloses that in this case, the conditional branch is predicted taken and a one is shifted into the register. Column 13, lines 19-21. Zuraski further discloses that row C of Figure 4 shows the contents after execution of the conditional branch. Column 13, lines 21-22. Hence, Zuraski discloses shifting a "1" in the shift register if the conditional branch is taken and shifting a "0" in the shift register if the conditional branch is not taken. However, Zuraski does not append a bit of a value to a vector when a fetch group has at least one branch instruction predicted to be a branch taken. Thus, Zuraski does not disclose all of the limitations of claim 6, and thus Zuraski does not anticipate claim 6. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "appending a bit of a second value to the first vector when the first group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken" as recited in claim 6. The Examiner cites column 12, lines 38-42; column 13, lines 7-36; Figures 4 and 5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 4. Applicant respectfully traverses. As stated above, Zuraski instead discloses that a taken branch is indicated by a binary one and a not taken branch is indicated by a binary zero. Column 13, lines 12-14. Zuraski further discloses that row A of Figure 4 shows the contents prior to dispatch of a conditional branch. Column 13, lines 17-18. Zuraski further discloses that row B of Figure 4 contains the contents after dispatch of a single conditional branch. Column 13, lines 18-19. Zuraski further discloses that in this case, the conditional branch is predicted taken and a one is shifted into the register. Column 13, lines 19-21. Zuraski further discloses that row C of Figure 4 shows the contents after execution of the conditional branch. Column 13, lines 21-22. Hence, Zuraski discloses shifting a "1" in the shift register if the conditional branch is taken and shifting a "0" in the shift register if the conditional branch is not taken. However, Zuraski does not append a bit of a value to a vector when the fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken. Thus, Zuraski does not disclose all of the limitations of claim 6, and thus Zuraski does not anticipate claim 6. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "retain a current vector in said shift register when a selected fetch group does not contain at least one branch instruction" as recited in claim 17. The Examiner cites column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67 and Figure 1 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 9. The Examiner further states that "maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch." Paper No. 7, page 9. Applicant respectfully traverses the implied assertion that Zuraski inherently discloses retaining a current vector stored in the shift register when a selected fetch

group does not contain at least one branch instruction. As stated above, Zuraski does not disclose selecting a fetch group. Applicant respectfully points out that the Examiner must provide a basis in fact and/or technical reasoning to assert that Zuraski inherently discloses retaining a current vector stored in the shift register when a selected fetch group does not contain at least one branch instruction. *Ex parte Levy.* 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, in order for the Examiner to establish inherency, the Examiner must provide extrinsic evidence that must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherency, however, may not be established by probabilities or possibilities. *Id.* The mere fact that a certain thing may resolve from a given set of circumstances is not sufficient. *Id.* Therefore, the Examiner must support her inherency argument with objective evidence meeting the above requirements. Since the Examiner has not provided any objective evidence in support of her inherency argument, the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 17. M.P.E.P. § 2141.

Claims 2-5, 7-12, 14-16, 18 and 20 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above stated reasons. Claims 2-5, 7-12, 14-16, 18 and 20 recite additional features, which, in combination with the features of the claims upon which they depend are not anticipated by Zuraski.

For example, Zuraski does not disclose "storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions" as recited in claim 2. The Examiner cites to column 10, lines 5-6 and Figure 3 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 3. Applicant respectfully traverses and asserts that Zuraski discloses that the global history shift register is coupled to line buffer 210. However, there is no language in the cited passage that discloses that the value generated based on whether a group of instructions includes or does not include a branch instruction predicted as taken is

stored in line buffer 210. Thus, Zuraski does not disclose all of the limitations of claim 2 and thus Zuraski does not anticipate claim 2. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "correcting the generated vector upon a misprediction comprising the substeps of: retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register; and shifting an updated history bit into the shift register" as recited in claim 3. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 3. Applicant respectfully traverses and asserts that Zuraski instead discloses that line buffer 210 entry is used to update or repair the branch prediction and global history upon retirement or misprediction. Column 10, lines 49-51. Zuraski further discloses that in the case of a mispredicted branch, the global history register is updated by modifying the history bit representing the mispredicted branch from a binary one to a zero. Column 13, lines 34-36. Hence, Zuraski does not disclose shifting an updated history bit into the shift register. Instead, Zuraski discloses modifying the history bit to be a different logic value. Further, while Zuraski discloses that line buffer 210 entry is used to update or repair the branch prediction and global history upon retirement or misprediction, the Examiner has not cited to any passage in Zuraski that discloses retrieving a selected number of bits of a vector stored in line buffer 210 into the shift register. Thus, Zuraski does not disclose all of the limitations of claim 3, and thus Zuraski does not anticipate claim 3. M.P.E.P. §2131.

Furthermore, with respect to the above-cited claim rejection, Zuraski instead discloses restoring the state of the register at the time of prediction of the first conditional branch with the history changed from a binary one to a binary zero to reflect the not taken branch. Column 13, lines 50-53. Zuraski further discloses that the history of the second conditional branch is no longer present in the history register as it represents an erroneous instruction stream. Column 13, lines 53-56. Zuraski further discloses that in this case it was necessary to right-shift the history in the register and restore the history of a branch which was previously left-shifted out.

Column 13, lines 56-58. Again, Zuraski discloses modifying the history bit representing the mispredicted branch from a binary one to a zero. Zuraski does not disclose shifting an updated history bit into the shift register but instead discloses right-shifting the history in the register and restoring the history of a branch which was previously left-shifted out. Thus, Zuraski does not disclose all of the limitations of claim 3, and thus Zuraski does not anticipate claim 3. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "wherein the selected group of instructions comprises eight instructions" as recited in claim 5. The Examiner cites column 12, lines 38-42; column 13, lines 7-36 and Figures 4-5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 4. Applicant respectfully traverses and asserts that Zuraski instead discloses an 8 bit global history shift register. However, while the register is an 8 bit register, there is no language in the cited passages that discloses determining if a selected group of instructions contains a branch instruction where the selected group of instructions comprises eight instructions. Hence, there is language in the cited passage that discloses determining if a branch instruction is contained in a group of eight instructions. Thus, Zuraski does not disclose all of the limitations of claim 5 and thus Zuraski does not anticipate claim 5. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "storing the first and second vectors in an entry of a branch history queue associated with the first fetch group" as recited in claim 7. The Examiner cites to column 10, lines 5-6 and Figure 3 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski discloses that the global history shift register is coupled to line buffer 210. However, there is no language in the cited passage that discloses that the vectors generated based on whether a fetch group contains or does not contain a branch instruction predicted to be a branch taken is stored in line buffer 210. Thus, Zuraski does not disclose all of the limitations of claim 7 and thus Zuraski does not anticipate claim 7. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "detecting a branch misprediction based on the first prediction value" as recited in claim 8. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages of detecting a branch misprediction based on a prediction value that was retrieved from a branch history table. The Examiner had previously asserted that global predictor storage 205 teaches a branch history table. Paper No. 7, page 4. However, there is no language in the cited passages that a prediction value from global predictor storage 205 is used to detect a branch misprediction. Thus, Zuraski does not disclose all of the limitations of claim 8 and thus Zuraski does not anticipate claim 8. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "retrieving the first and second vectors from the branch history queue" as recited in claim 8. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages that discloses retrieving vectors from a branch history queue. Thus, Zuraski does not disclose all of the limitations of claim 8 and thus Zuraski does not anticipate claim 8. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "indexing the branch history table using the first vector to correct the first prediction value" as recited in claim 8. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages of indexing a branch history table using a vector to correct a prediction value. The Examiner had previously asserted

that global predictor storage 205 teaches a branch history table. Paper No. 7, page 4. However, there is no language in the cited passages that discloses indexing in global predictor storage 205 using a vector to correct a prediction value. Thus, Zuraski does not disclose all of the limitations of claim 8 and thus Zuraski does not anticipate claim 8. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "appending a corrected bit to the second vector to generate a corrected branch history vector" as recited in claim 8. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski instead discloses that the global history register is updated by modifying the history bit representing the mispredicted branch from a binary one to a zero in the case of mispredicting a conditional branch to be taken instead of not taken. Zuraski illustrates modifying the history bit from a binary one to a zero in Figure 5. Hence, discloses replacing one value with another value in the case of a misprediction. However, Zuraski does not disclose appending a corrected value to the vector in the global history register. Thus, Zuraski does not disclose all of the limitations of claim 8 and thus Zuraski does not anticipate claim 8. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "wherein said fetch cycle precedes the second fetch cycle by three fetch cycles" as recited in claim 9. The Examiner cites column 1, lines 13-20 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 5. Applicant respectfully traverses and asserts that Zuraski instead discloses that a clock cycle refers to an interval of time accorded to various stages of an instruction processing pipeline within the microprocessor. The language in the cited passage is not specific as to a number of fetch cycles. Neither is there any language in the cited passage disclosing a number of three fetch cycles between a first fetch cycle (used to retrieve a first prediction value) and a second fetch cycle (used to retrieve a second prediction value). Thus, Zuraski does not disclose all of the limitations of claim 9 and thus Zuraski does not anticipate claim 9. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "wherein said substeps of appending comprise the substeps of shifting a bit into a shift register storing the second vector" as recited in claim 12. The Examiner cites column 12, lines 38-42; column 13, lines 7-36 and Figures 4-5 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 6. Applicant respectfully traverses. As stated above, Zuraski instead discloses that the global history register is updated by modifying the history bit representing the mispredicted branch from a binary one to a zero in the case of mispredicting a conditional branch to be taken instead of not taken. Zuraski illustrates modifying the history bit from a binary one to a zero in Figure 5. Hence, discloses replacing one value with another value in the case of a misprediction. However, Zuraski does not disclose shifting a corrected value to the vector in the global history register. Thus, Zuraski does not disclose all of the limitations of claim 12 and thus Zuraski does not anticipate claim 12. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "a queue for storing said first and said second vectors" as recited in claim 15. The Examiner cites to column 10, lines 5-6 and Figure 3 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 7. Applicant respectfully traverses and asserts that Zuraski discloses that the global history shift register is coupled to line buffer 210. However, there is no language in the cited passage that discloses that the vectors generated based on whether a group of instructions contains or does not contain a branch instruction predicted to be a branch taken is stored in line buffer 210. Thus, Zuraski does not disclose all of the limitations of claim 15 and thus Zuraski does not anticipate claim 15. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "accessing said vectors from said queue" as recited in claim 15. The Examiner cites column 10, lines 5-6 and 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 7. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages that discloses accessing vectors from a queue. Thus, Zuraski does not

disclose all of the limitations of claim 15 and thus Zuraski does not anticipate claim 15. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "indexing said branch history table with said first vector and updating a corresponding entry with a corrected prediction value" as recited in claim 15. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 8. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages of indexing a branch history table using a vector and updating an entry with a corrected a prediction value. The Examiner had previously asserted that global predictor storage 205 teaches a branch history table. Paper No. 7, page 4. However, there is no language in the cited passages that discloses indexing in global predictor storage 205 using a vector and updating an entry in global predictor storage 205 with a corrected prediction value. Thus, Zuraski does not disclose all of the limitations of claim 15 and thus Zuraski does not anticipate claim 15. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "updating a vector in said shift register with said second vector" as recited in claim 15. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 8. Applicant respectfully traverses and asserts that Zuraski instead discloses that the global history register is updated by modifying the history bit representing the mispredicted branch from a binary one to a zero in the case of mispredicting a conditional branch to be taken instead of not taken. Zuraski illustrates modifying the history bit from a binary one to a zero in Figure 5. Hence, discloses replacing one value with another value in the case of a misprediction. However, Zuraski does not disclose updating a vector in a shift register with another vector that was generated by shifting a value into the shift register when the group of instructions contains a branch instruction and does not contain a branch instruction predicted as a branch taken.

Thus, Zuraski does not disclose all of the limitations of claim 15 and thus Zuraski does not anticipate claim 15. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "shifting the corrected prediction value into said shift register" as recited in claim 15. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 8. Applicant respectfully traverses and asserts that Zuraski instead discloses that the global history register is updated by modifying the history bit representing the mispredicted branch from a binary one to a zero in the case of mispredicting a conditional branch to be taken instead of not taken. Zuraski illustrates modifying the history bit from a binary one to a zero in Figure 5. Hence, discloses replacing one value with another value in the case of a misprediction. However, Zuraski does not disclose shifting a corrected value into the shift register. Thus, Zuraski does not disclose all of the limitations of claim 15 and thus Zuraski does not anticipate claim 15. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "a branch instruction queue having a plurality of entries each associated with a fetch group for storing at least first and second corresponding global history vectors" as recited in claim 18. The Examiner cites column 10, lines 5-6 and Figure 3 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 10. Applicant respectfully traverses and asserts that Zuraski instead discloses a global shift register coupled to global predictor storage 205 and line buffer 210. However, there is no language as to line buffer 210 or global predictor storage 205 (Applicant is unsure as to which unit the Examiner alleges as disclosing a branch instruction queue) having a plurality of entries where each entry is associated with a fetch group. Further, there is no language in the cited passage of line buffer 210 or global predictor storage 205 (Applicant is unsure as to which unit the Examiner alleges as disclosing a branch instruction queue) storing global history vectors. Thus, Zuraski does not disclose all of the limitations of claim 18 and thus Zuraski does not anticipate claim 18. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "detecting a misprediction associated with a said prediction value retrieved from said branch history table and corresponding to said first global history vector in said branch instruction queue" as recited in claim 18. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 10. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages of detecting a branch misprediction based on a prediction value that was retrieved from a branch history table. The Examiner had previously asserted that global predictor storage 205 discloses a branch history table. Paper No. 7, page 4. However, there is no language in the cited passages that a prediction value from global predictor storage 205 is used to detect a branch misprediction. Thus, Zuraski does not disclose all of the limitations of claim 18 and thus Zuraski does not anticipate claim 18. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "retrieving said first vector from said branch instruction queue and accessing a corresponding entry in said branch history table to correct said prediction value stored therein" as recited in claim 18. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 10. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. However, there is no language in the cited passages of retrieving a vector from a branch instruction queue. Neither was there any language in the cited passages of accessing an entry in a branch history table to correct a prediction value stored therein. The Examiner had previously asserted that global predictor storage 205 discloses a branch history table. Paper No. 7, page 4. However, there is no language in the cited passages that an entry in global predictor 205 is accessed to correct a prediction value. Thus, Zuraski does not disclose all of the limitations of claim 18 and thus Zuraski does not anticipate claim 18. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "retrieving and modifying said second vector to generate a corrected vector in said shift register" as recited in claim 18. The Examiner cites column 10, lines 49-51; column 13, line 26 – column 14, line 5; and Figures 3, 5, 6 and 7 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 10. Applicant respectfully traverses and asserts that Zuraski instead discloses updating a global history register after a misprediction. There is no language in the cited passages of retrieving and modifying a vector from a branch instruction queue to generate a corrected vector in the shift register. Thus, Zuraski does not disclose all of the limitations of claim 18 and thus Zuraski does not anticipate claim 18. M.P.E.P. §2131.

Applicant further asserts that Zuraski does not disclose "wherein said fetch group comprises eight instructions" as recited in claim 20. The Examiner cites column 4, lines 12-19 of Zuraski as disclosing the above-cited claim limitation. Paper No. 7, page 10. Applicant respectfully traverses and asserts that Zuraski instead discloses a byte comprises 8 binary bits. This is not the same as a fetch group comprising eight instructions. Thus, Zuraski does not disclose all of the limitations of claim 20 and thus Zuraski does not anticipate claim 20. M.P.E.P. §2131.

As a result of the foregoing, Applicant respectfully asserts that not each and every claim limitation was found within the cited prior art reference, and thus claims 1-18 and 20 are not anticipated by Zuraski.

II. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner rejects claim 19 under 35 U.S.C. §103(a) as being unpatentable over Zuraski in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications Second Edition ©1987 (hereinafter "Rosenberg"). Applicant respectfully asserts that claim 19 is allowable as claim 17[1] is allowable for at least the reasons stated above.

[1] Applicant respectfully notes that claim 19 depends from independent claim 17.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicant that claims 1-20 in the Application are in condition for allowance, and Applicant respectfully requests an allowance of such claims. Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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